

## Review Article

# A Nanotechnology Enhancement to Moore's Law

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Intel Moore observed an exponential doubling in the number of transistors in every 18 months through the size reduction of transistor components since 1965. In viewing of mobile computing with insatiate appetite, we explored the necessary enhancement by an increasingly maturing nanotechnology and facing the inevitable quantum-mechanical atomic and nuclei limits. Since we cannot break down the atomic size barrier, the fact implies a fundamental size limit at the atomic/nucleus scale. This means, no more simple 18-month doubling, but other forms of transistor doubling may happen at a different slope. We are particularly interested in the nano enhancement area. (i) 3 Dimensions: If the progress in shrinking the in-plane dimensions is to slow down, vertical integration can help increasing the areal device transistor density. As the devices continue to shrink into the 20 to 30 nm range, the consideration of thermal properties and transport in such devices becomes increasingly important. (ii) Quantum computing: The other types of transistor material are rapidly developed in laboratories worldwide, for example, Spintronics, Nanostorage, HP display Nanotechnology, which are modifying this Law. We shall consider the limitation of phonon engineering fundamental information unit "Qubyte" in quantum computing, Nano/Micro Electrical Mechanical System (NEMS), Carbon Nanotubes, single-layer Graphenes, single-strip Nano-Ribbons, and so forth.

## 1. Introduction

There have been numerous papers and scientists' experiments about the lives and deaths of Moore's Law which are dealing with several technological issues and economics barriers. Indeed, looking at the history of integrated circuits from 1975 to 2011, a doubling of transistor counts every twenty-four months was a good estimation. This prediction, known as Moore's Law, has become a business dictum for the whole semiconductor industry. However, "what the Moore's Law is" and "how did it came about" are not clear. We observe that Moore's Law has expanded beyond its original intentions/meaning. The definition of Moore's Law has come to refer to almost anything related to the semiconductor industry that, when plotted on semilog paper, approximates a straight line [1].

In this work, by reviewing Moore's Law history, investigating possible barriers for Moore's Law, and predicting potential nanotechnologies to enhance Moore's Law, we define a roadmap of future key technologies. In addition, we

also estimate the end of Moore's Law, assuming we focus on technical capabilities.

## 2. Moore's Law History

Alan Turing in his 1950 paper [2] "Computing machinery and intelligence" had predicted that by the turn of the millennium, we would have "computers with a storage capacity of about  $10^9$ " what today we would call 128 megabytes processing speed, memory capacity, sensors, and even the number and size of pixels in digital cameras, for example, smartphone. After him, Gordon Earle Moore (born January 3, 1929; UC Berkeley BS Chemistry, 1950; Caltech PhD. major in Chemistry and minor Physics, 1954) is the cofounder and Chairman Emeritus of Intel Corporation. In 1965, Moore, a founder of Fairchild Semiconductor (later Intel), observed in his famous paper [3] that "the complexity for minimum component costs has increased at a rate of roughly a factor of two per year". Extrapolating this trend for a decade,

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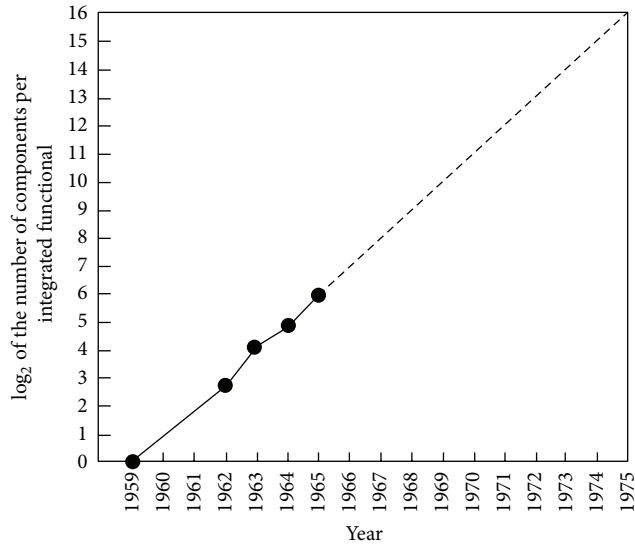


FIGURE 1: Moore's prediction, in 1965, of the doubling of the number of minimum cost components on a chip per year, with extrapolated to 1975 [3].

Moore predicted that chips with 65,000 components would be available by 1975. This observation of exponential growth in circuit density has proven to be one of the greatest examples of prescience in modern era.

Moore then refined his component count estimation, in 1975, to a doubling every twenty-four months, and thus a reduced exponential growth compared to his initial estimation in 1965 [4]. Based on the history of integrated circuits from 1975 to 2008, a doubling of transistor counts every two years was a good estimation.

This prediction known as *Moore's Law* has become a remarkable evolutionary trend for the whole semiconductor industry.

Indeed, Moore himself already observed, in 1995, that the semiconductor industry cannot continue its fast exponential growth indefinitely, since it would exceed the gross world product (GWP) at some time. In the meantime, lots of publications deal with technological limitations to Moore's Law, for example, [5].

### 3. Current Barrier of Moore's Law

Gordon Moore's prediction is that the density of transistors and computing power doubles every twenty-four months, which has held since there were fewer than 100 transistors in an integrated circuit. Up to today's many millions of transistors on a single-integrated computer chip are still followed this trend. This amazing prediction has encouraged some authors to state that "periodically, people predict the death of Moore's Law. They state that Moore's Law eventually will end because of some future technological or scientific barrier. However, to date, engineers and scientists have found a way around these problems, and Moore's Law continues to be an accurate means of predicting the future development of technology" [6].

In this paper, we discuss the possible barrier of Moore's Law then follow by the possible technologies that may enhance Moore's Law.

**3.1. Performance Demand of Processor.** Intel CTO Justin Rattner recently stated in an interview with Network World that Moore's Law will likely be the rule for many decades to come. "If Moore's Law is simply a measure of the increase in the number of electronic devices per chip, then Moore's Law has much more time to go, probably decades"; he is quoted as saying.

Figure 2 shows the technology node from 130 nm to 22 nm announced recently versus the performance of the semiconductor chips. The gate length keeps on shrinking as the technology node decreases. As what most people expected for past few decades, the performance or the speed of the designed semiconductor chips should be increased as well. However, we can observe from this figure that the performance was, in contrast, decreased after technology node reached 65 nm.

The major reasons for this result are mainly from the following: current leakage, power consumption, and heat sink. These factors will limit the modern consumer demand products such as smartphone, laptop, and flat-panel device.

The drivers for technology development fall into two top-level categories: push and pull. As the electronics have grown to become a \$2 trillion USA industry as well as an enabler for productivity and growth in all areas of economic activity, the mobile devices are obviously the major push drivers for the economic. However, these push drivers, in contract, become the pull drivers for performance of the semiconductor chips due to the following major factors: low cost, mobility, and low power. First of all, the major characters of modern mobile devices are huge amount of end user and short recycle time. This will limit the unit cost of the mobile device. Hence, the cost of research and development, manufacture, texting, and packing will also be limited. Secondly, the other character of modern mobile devices is mobility. This will limit the weight of the mobile device. However, it increases the requirements for wireless communication module, such as WiFi, Bluetooth, GPS, and 3G/4G communication, inside these devices. Therefore, a complex tradeoff between cost, weight, and performance will need to be seriously considered in modern mobile device industry. In other words, when we discuss Moore's Law, it is not just simply a measure of the increase in the number of electronic devices per chip.

**3.2. Power Source/Consumption and Heat Sink.** As mobile device industry keeps growing up, energy is always one of the most important issues in this century. Therefore, research and development of new energy storage materials and devices are receiving worldwide concern and increasing research interest [7]. Graphene, a unique two-dimensional carbon material, is predicted to be an excellent electrode material candidate for energy conversion/storage systems because of its high-specific surface area, good chemical stability, excellent electrical, and thermal conductivity as well as remarkably high mechanical strength and Young's modulus.

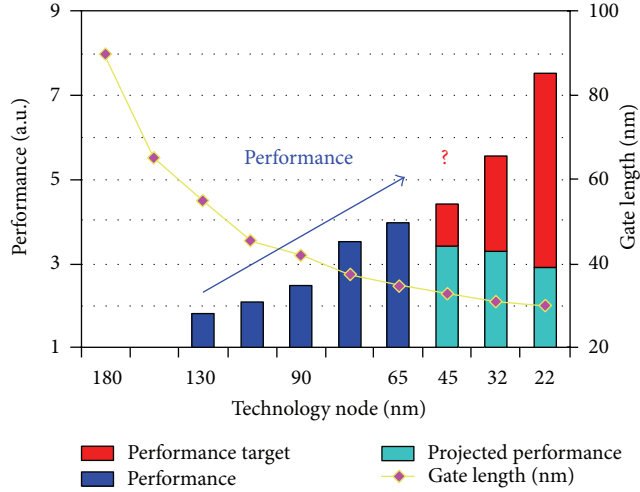


FIGURE 2: Performance demand of processor [5].

Indeed, increasing the battery performance can provide more room for the performance of processor. However, the generated heat will become another barrier for the mobile device development, especially for the smartphone, flat-panel PC, and Ultra-Book which do not allow a build-in fan structure. These limitations will become another factor to further limit Moore's Law in the future.

**3.3. Tunneling Effect.** Semiconductor manufacturers will be able to produce chips on the 14 nm manufacturing process, expected by conservative estimates to arrive in 2018. However, semiconductor makers will not be able to shrink transistors much, if at all, beyond 2021, according to a new paper from Intel [8]. Transistors are essentially microscopic on/off switches that consist of a source (S), where electrons come from, a drain (D), where the electrons target to, and a gate (G) that mainly controls the flow of electrons through a channel that connects the source and the drain. When the length of the gate gets smaller than 5 nanometers, however, tunneling effect will begin to kick into play. Electrons will simply pass through the channel on their own without any driver voltage, because the source and the drain will be extremely close. Therefore, a transistor becomes unreliable as a source of basic data, because the probability of spontaneous transmission is about 50 percent. In other words, Heisenberg's uncertainty principle is in action, because the location of the electrons cannot be accurately predicted based on Heisenberg's uncertainty principle.

On a two-year cycle based on Moore's Law, this would mean that 16-nanometer chips would appear in 2013 with the barriers preventing new, smaller chips in 2015.

Semiconductor manufacturers, however, have had to delay the introduction of new processes recently, around 2012. Using a three-year calendar, 5-nanometer chips will not hit until 2018 or 2019 based on the new technology progress update history, putting a barrier generation at about 2021. The ITRS timetable will provide more details about the different manufacturing technologies for a given year.

However, the tunneling effects will occur regardless of the chemistry of the transistor materials. Several researchers over the years have predicted the end of Moore's Law but made the mistake of extrapolating on the basis of existing materials.

**3.4. The Quantum Limit to Moore's Law.** Gordon Moore himself stated during an interview September 18, 2007, at Intel's twice-annual technical conference that we will soon be bumping against the laws of physics: "another decade, a decade and a half I think we'll hit something fairly fundamental."

Since this involves a physics limit (in his words), he went on to quote Stephen Hawking during his visit to Intel in 2005. "When Stephen Hawking was asked what are the fundamental limits to microelectronics, he said the speed of light and the atomic nature of matter" [9]. Determining an ultimate physics limit to Moore's Law would mark out a future boundary to electronics miniaturization.

A calculation of the quantum limit to Moore's Law was conducted by writing Moore's Law in equation form as [5]

$$n_2 = n_1 2^{[(y_2 - y_1)/2]} \quad (1)$$

This equation predicts the number  $n_2$  of transistors or equivalent computing power in any given year  $y_2$  from the number  $n_1$  of transistors in any other earlier year  $y_1$  [5].

From the definition of Moore's Law, we know that the characteristic dimension or length  $L$  of a transistor is inversely proportional to the number of transistors  $n$  on an IC. If the measurement of  $n$  is in "number per meter," then, from dimensional analysis, the measurement of  $L$  is in meters (m), or, equivalently,  $1/L$  is the number per meter just as in (1).

We can then rewrite (1) as

$$\frac{1}{L_2} = \left( \frac{1}{L_1} \right) 2^{[(y_2 - y_1)/2]} \quad (2)$$

The characteristic dimension of an electron from Heisenberg uncertainty is the Compton wavelength [10]  $\lambda_c = h/m_e c = 2.4263 \times 10^{-12}$  m based on Planck's constant  $h$ , the mass of the electron  $m_e$ , and the speed of light  $c$ .

The Compton wavelength of the electron is the fundamental limit to measuring its position based on quantum mechanics and special relativity, or the length scale where a relativistic quantum field theory is necessary for an adequate description [11]. The Compton wavelength is therefore the fundamental boundary to determining the position (or spin) of a particle, which satisfies the Stephen Hawking prediction that this limit would be based on the speed of light and the atomic nature of matter since  $c$  is determined by  $\lambda_c$ ,  $m_e$ , and  $h$  [5]. Rewriting (2) using the year of 2008 with available technology, transistor feature size, and Compton wavelength,  $2.4263 \times 10^{-12}$  m or 0.00243 nm:

$$(2.4263 \times 10^{-12} \text{ m})^{-1} = (0.045 \times 10^{-6} \text{ m})^{-1} 2^{[(y_2 - 2008)/2]} \quad (3)$$

Solving for the exponent  $\Delta y = (y_2 - 2008)$  using the natural log function, we end up to have

$$y_1 = 28.36y + 2008 = \text{year 2036.} \quad (4)$$

This is the quantum limit year predicted by Moore's Law if electrons were implemented as the smallest quantum computing transistor elements [5].

**3.5. The Economic Limit to Moore's Law.** The higher component density has led to a decrease in end consumer prices. However, the costs for producers follow a converse trend: research and development, manufacture, and tests become more and more expensive with each new generation. This observation is known as *Rock's Law* and sometimes also referred to as Moore's Second Law [12]; fabrication facility (fab) costs also follow an exponential growth. Despite this exponential growth of facility costs, the cost per shipped unit decreases at an exponential rate. Karl Rupp first investigated economic limitations to the semiconductor business. A summary of their results has already been published in [13]. Karl then found out If costs for a single fab are at most 0.02% of the GWP (i.e.,  $\epsilon = 0.0002$ ), a reduced growth of transistor counts per chip for economic reasons is likely to happen around 2020 as shown in Figure 3.

**3.6. On-Board Limit to Moore's Law.** There have been numerous papers and discussions about the lives and deaths of Moore's Law, all of them dealing with several technological questions inside semiconductor chip. However, any semiconductor chip cannot exist along without PCB board, no matter flexible or not.

Higher bandwidth has become more important than ever in today's computing systems. Personal computers, routers, switches, and game consoles all require higher bandwidth to meet the increasing performance demand of new applications. Moreover, the continuous scaling of integrated circuit technology, confirming Moore's prediction, over the recent years has resulted in massive computational capacity and hence data processing capability which in turn has created the demand for high-speed communication across different components in a system [14]. These systems extend to optical communication networks spanning across the globe, but all come down to chip-to-chip communication in a single board [15]. The massive flux of information in and out of the chip has caused simple input/output (I/O) drivers to be replaced with sophisticated high-speed circuits which in turn depend on reliable high bandwidth channels.

Channel design, which was conveniently and justifiably ignored at lower frequencies, has become a major bottleneck for high-speed communication. The increase in data rates to the tens of Giga bits per second (Gbps) region has prompted more careful signal integrity considerations in the design of the channel from the transmitter of one chip to the receiver on the next. The decrease in wavelength size due to higher frequency signaling has caused the once short electrical lengths of different components to become significant due to transmission line delays, loss, and signal coupling in these components [16].

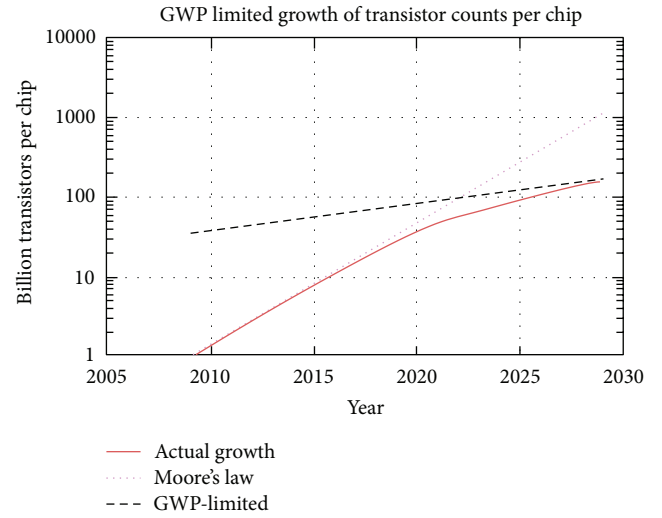


FIGURE 3: If costs for a single fab are at most 0.02% of the GWP (i.e.,  $\epsilon = 0.0002$ ), a reduced growth of transistor counts per chip for economic reasons is likely to happen around 2020 [13].

Therefore, on-board transmission line would become a remarkable bottleneck for the input/output of the semiconductor design.

In addition, another possible on-board barrier would be on the other end of the transmission line as we discussed above, that is, the state-of-the-art analog to digital conversion (ADC) devices.

ADC devices translate physical information into a stream of numbers, enabling digital processing by sophisticated software algorithms. The ADC task is inherently intricate: its hardware must hold a snapshot of a fast-varying input signal steady, while acquiring measurements. Since these measurements are spaced in time, the values between consecutive snapshots are lost. In general, therefore, there is no way to recover the analog input unless some prior on its structure is incorporated [17]. A common approach in engineering is to assume that the signal is bandlimited, meaning that the spectral contents are confined to a maximal frequency  $f_{\text{max}}$ . Bandlimited signals have limited (hence slow) time variation and can therefore be perfectly reconstructed from equispaced samples with a rate at least 2 times  $f_{\text{max}}$ , termed the Nyquist rate. This fundamental result is often attributed in the engineering community to Shannon-Nyquist [18].

Uniform sampling ADC devices are the most common technology in the market. Figure 4 maps off-the shelf ADC devices according to their sampling rate. The ADC industry has perpetually followed the Nyquist paradigm—the datasheets of all the devices that are reported in the figure highlight the conversion speed, referring to uniform sampling of the input. The industry is continuously striving to increase the possible uniform conversion rates.

Therefore, the ADC devices on the user input/output sides could become another possible barrier of the semiconductor design. This barrier may happen sooner when the higher quality of video and audio is demanded as well as



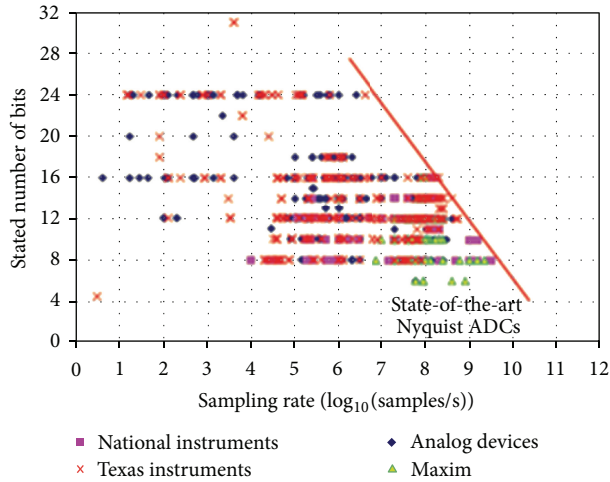


FIGURE 4: ADC technology: stated number of bits versus sampling rate. A map of more than 1,200 ADC devices from four leading manufacturers, according to online datasheets [17].

the higher speed requirement for wireless communication of mobile device such as smartphone, flat-panel PC, and laptop.

**3.7. Mobile Device-Driven Industry.** With the developing of the mobile devices, especially smartphones and multimedia Mobile (MMM) phones, more functionalities, faster download speed are becoming the main demands of customers. As the result, mobile market does not only depend on better hardware but also matter of bandwidth and frequencies. It is shown in Figure 5 below that mobile bandwidth (TB per month) grows extremely fast since 2011 [19]. We can find that different media share the whole bandwidth usage. So the sharing and cross talk among billions of users require bandwidth sharing strategies.

In addition, video will account for 64% of mobile traffic by 2013 and mobile data traffic will be more than double every year through 2013. In 2013, most important, mobile data traffic will be more than 66 times greater than mobile data traffic in 2008.

With the fast development of new technology, electronic devices tend to be smaller and more efficient. The market developed from PC to laptop and palm, all the way to cell phone and smart phone. Mobile devices, such as smartphone and tablet computers, are becoming more popular than ever. In most countries, the occupation ratio of mobile device is much higher than that of PC. As shown in Figure 6, global Internet users will double over the next few years, most of which will be mobile devices [20].

Due to the global Internet devices sales research, in a few years, the number of the mobile devices will dwarf the number of PCs. It is shown in Figure 7 that PC sales curve will become flat few years later, while smartphone and tablet sales will go up straight to the top [21].

The total global mobile phone market is expected to be worth \$341.4 billion by 2015, while smartphone will occupy 75.8% of the overall mobile sales market in the same year.

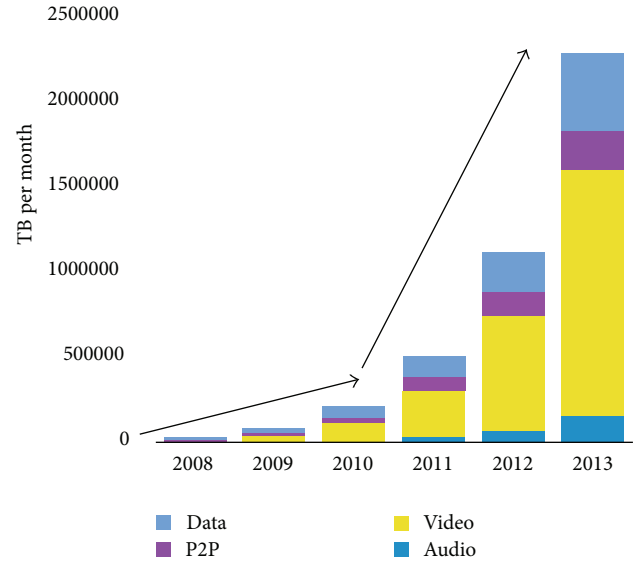


FIGURE 5: Mobile device bandwidth trend.

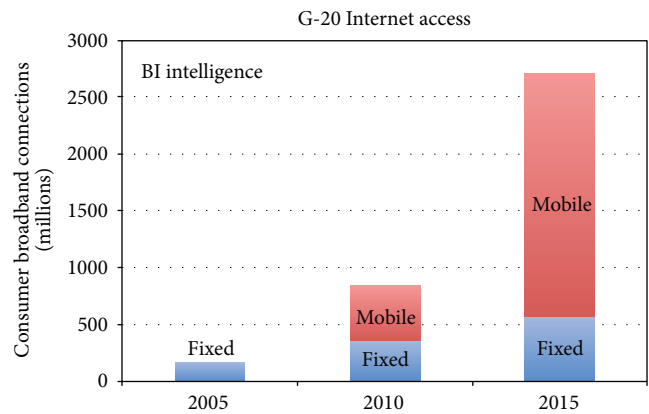


FIGURE 6: Global Internet connections in million.

However, the fast development of mobile devices will have impact on Moore's Law, which is a crucial factor in electronic manufactory fields. What is actually happening is that there is a race for mobile devices market in demand now versus the realities of Moore's Law. The law which states that the number of transistors that can be placed inexpensively on an integrated circuit doubles approximately every two years, and the performance will double in the same period. This law has remained true over the last 40 years, driven the technology industry, and has enabled computing devices to get cheaper, smaller, and more powerful and hence deliver more functionality. By prediction, Moore's Law will not remain fully precise in next decades due to the restriction of power consumption, size, and price.

**3.7.1. Mobile Device-Driven Industry: Size/Weight.** Today, mobile device is becoming smaller and lighter to meet the users' requirements and the most advanced logic technology node in production is 22 nm in 2012 and the target for

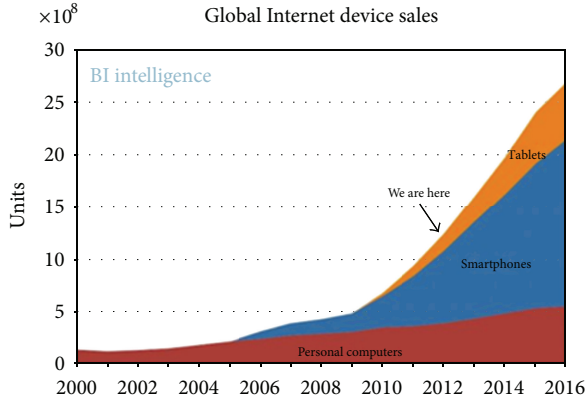


FIGURE 7: Global Internet device sales.

2013 will be 14 nm. With feature sizes below 100 nm, silicon technology has entered the realm of nanotechnology and continuing true Moore's Law becomes more and more difficult and requires new structures, materials, and technology.

The three important factors to reduce size are lithography, scalability of the planar CMOS transistor, and performance degradation due to pitch scaling. But we can predict that the trend of pitch will slow and stop during the next 10 years because the size cannot be half separated infinitely due to the physical rules. Addressing the lithography tool roadmap here, the classical pitch size for a given lithography single exposure is a straight-forward consequence of the diffraction-limited resolution of the projection optics. The lateral optical resolution is given by the quotient of the illumination wavelength,  $\lambda$ , and the numerical aperture, NA, of the projection optics according to the famous Rayleigh formula  $\Delta x = k_1(\lambda/NA)$ , where  $k_1$  is a process factor determined by the exact details of the optical system.

In the past years, each of these factors has been addressed to increase the attainable resolution of a photolithography system and finally reached their limitations [22]. To pattern finer pitch, the industry solution is now either double patterning or DUV. However, for double patterning, it will cost extra processing challenging when smaller than 22 nm, which results in a cost issue. Also, for DUV (deep-UV) method, it has approached a technology limit of 193 nm [23]. As a result, Moore's Law will not be continuing forever due to these limitations.

**3.7.2. Mobile Device-Driven Industry: Market Price.** As discussed above in Section 3.5, smaller size will cause cost issues. At the same time, to secure the market of mobile devices, economic factors must be considered for each vendor. This means that if cost continues to grow for cooler functionalities, the growing market price will limit the development predicted by Moore's Law. This is because there is a relationship between supply and demand in economic area. For example, if price increases, the number of consumers will decrease, and then the number of products will reduce. In his research, as discussed in Section 3.5, Karl Rupp pointed out that Moore's Law would be slowed down due to the limitation of GWP (gross world product) around 2020, as shown in Figure 3.

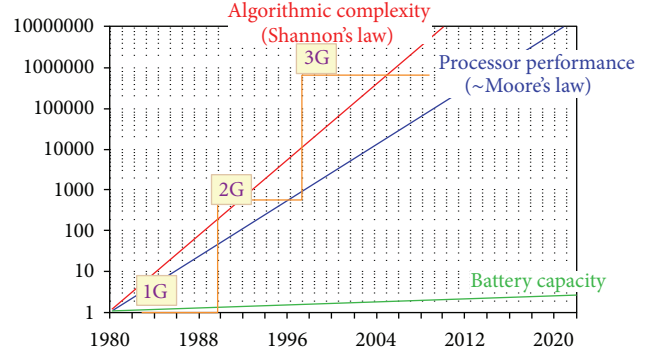


FIGURE 8: Shannon's Law versus Moore's Law.

**3.7.3. Mobile Device Driven Industry: Power Consumption and Shannon's Law.** According to Moore's Law, the size of transistor should be half every 2 years as discussed above. But when getting minimized, the physical characters will be changed a lot for nanoscale transistors. It will introduce a lot of new leakage mechanisms such as gate tunneling leakage, junction tunneling leakage, and subthreshold leakage. In this situation, to control the leakage power and dynamic power, power management IC will be introduced to SoC [24]. It is inferred here that the total number of functional transistors will not be to double due to the involved power management circuit.

For mobile system, the freedom fully depends on the energy provided by the batteries. As batteries can store a fixed amount of energy, the devices' operation time is limited as well [25] and the operation time becomes a significant factor for users because of the crammed up functionalities. So the main limiting factor in many portable device designs is not hardware or software, but instead how much power can be delivered by a battery.

However, research [26] states that although in the past 20 years system power consumption stays the same in every transistor-double technology generation cycle, in the next 20 years, power consumption will become a critical issue which will limit transistor's performance. As a result, if we use power management technology to reduce power consumption, as discussed above, the total number of functional transistors will not be doubled. If we do not use low-power design to solve this issue, then the fact that battery energy capacity for a given volume doubles only once per decade, as shown in Figure 8, will conflict with Moore's Law. In a word, no matter which solution we choose, it will make Moore's Law trend goes down in the future.

Figure 8 summarizes the key challenges facing the mobile device industry, which describes the gap among algorithmic complexity, processor performance, and the prediction of battery capacity. Algorithmic complexity, which is defined by Shannon's Law, tells the maximum rate at which information can be transmitted over a communications channel of a specified bandwidth in the presence of noise. It predicts that the transmission performance improves two times in 8.5 months, while processor performance improves two times in 18 months. In addition, it takes battery makers 5 to 10 years to achieve comparable increase in power density.

TABLE 1: Cellular system: 1G to 4G.

Decade	Generation	Efficiency: bps/Hz/sector
1980s	1G Analog cellular	0.016
1990s	2G Digital (TDMA → CDMA)	0.05 → 0.2
2000s	3G Enhanced CDMA	0.4 → 0.6
2010s	4G OFDM/MIMO	>1.0

To discuss the characteristics of mobile bandwidth, Nyquist-Shannon sampling theorem describes a worldwide sampling method in relation to bandwidth and frequency. The theorem states as if a function  $x(t)$  contains no frequencies higher than bandwidth  $B$  Hz, it is completely determined by giving its ordinates at a series of points spaced  $1/(2B)$  seconds apart. It is now used by mainstream information technology such as world's famous Code Division Multiplex (CDMA), the Orthogonal Frequency Division Multiplex (OFDM) with Multiple Input Multiple Output (MIMO). CDMA, which in one of several manifestations has been chosen for virtually all third-generation cellular systems, and OFDM with MIMO, which seems to be the most favored for a future generation [27].

CDMA is a spread spectrum multiple-access technique which spreads the bandwidth of the data uniformly for the same transmitted power and spread spectrum uses a transmission bandwidth that is several orders of magnitude greater than the minimum required signal bandwidth. OFDM is a method of encoding digital data on multiple carrier frequencies with all the carrier signals being orthogonal to each other. The orthogonality also allows high spectral efficiency, with a total symbol rate near the Nyquist rate for the equivalent baseband signal as compared in Table 1.

Although most of nowadays technologies are following Nyquist-Shannon sampling theorem, the theorem itself is meeting its limitation in regard with Moore's law. In fact, with the increasing data capacity and bandwidth, the number of I/O will grow with the sampling theorem which has a different speed with Moore's Law. The increasing size of the Shannon-Moore gap with time means that incremental transistors and MHz alone are not sufficient to close the gap between them. Furthermore, it is shown in Figure 9 below that if bandwidth capacity develops with Nyquist-Shannon sampling theorem, it will be hard to meet customers' demand [28].

A conclusion can be drawn from above that Nyquist-Shannon sampling theorem is increasingly incommensurate the technology demand. In this situation, compressed sensing, an alternative to Shannon/Nyquist sampling for acquisition of sparse or compressible signals that can be well approximated by just  $K \ll N$  elements from an  $N$ -dimensional basis. Instead of taking periodic samples, it measures inner products with  $M < N$  random vectors and then recovers the signal via a sparsity-seeking optimization or greedy algorithm [27]. So compressed sensing just obtains few compressed sparse sensing information of the sampling signals. At the same time, the sensing wave, unlike CDMA or OFDM, is irrelevant to the sparse space of signals. These characteristics will make I/O reduced compared to the

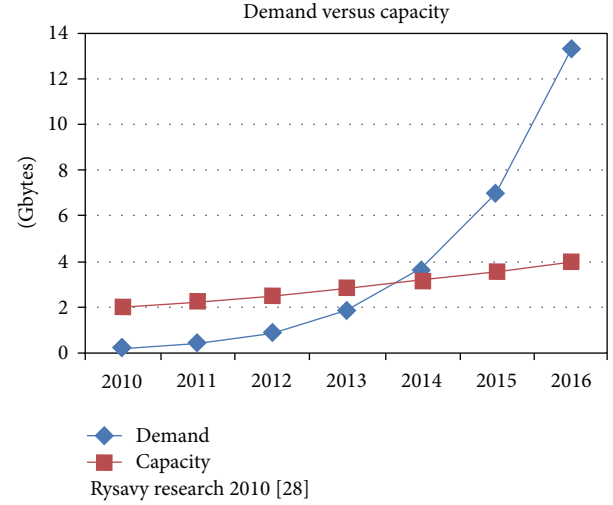


FIGURE 9: Average demand per user versus average capacity per user.

Shannon-Nyquist sampling and will also fit Moore's Law. As a result, the impact on Moore's Law which is due to Shannon-Nyquist theory will be eliminated.

#### 4. Nanoenhancement to Moore's Law

**4.1. DNA Scaffolding Tiny Circuit Board.** As what we discussed previously, any semiconductor chip cannot exist along without PCB board, no matter flexible or not. Due to the on-board transmission line effect for high speed communication, its the time for us to start thinking about new materials for the circuit board.

IBM researchers, working with the California Institute of Technology, claimed they have collaborated in combining lithographic patterning with self-assembly to devise a method of arranging DNA "origami" structures on surfaces compatible with current semiconductor manufacturing equipment. IBM's developed chip-building technology that uses a DNA-like structure as a "scaffold." As shows in Figure 10, low concentrations of triangular DNA origami are binding to wide lines on a lithographically patterned surface, built by IBM scientists.

This technology could be a major breakthrough in enabling the semiconductor industry to pack more power and speed into tiny computer chips, while making them more energy efficient and less expensive to manufacturer.

As we discussed previously in this paper, the semiconductor industry is faced with the challenges of developing lithographic technology for feature sizes smaller than 22 nm and exploring new classes of transistors that employ carbon nanotubes or silicon nanowires. IBM's approach of using DNA molecules as scaffolding—where millions of carbon nanotubes could be deposited and self-assembled into precise patterns by sticking to the DNA molecules—may provide a way to reach sub-22 nm lithography [29]. The cost involved in shrinking features to improve performance is a limiting factor in keeping pace with Moore's Law and a concern across the semiconductor industry.





FIGURE 10: IBM tiny circuit boards [14].

**4.2. 3D Tri-Gates Transistor.** For more than four decades, Intel has delivered the challenge of Moore's Law. However, a fundamental barrier which is emerging technology is approaching atomic dimensions. Intel is already working on technologies to overcome this.

Intel shrank the fabrication process to use 22 nanometer (nm = billionths of a meter) nodes. Next, Intel departed from traditional planar (2-D) gates, using instead 3-D Tri-Gate technology. Let us look at the reduction in circuit size first. In order to double the number of transistors, scientists need the fabrication process to use 22 nm nodes, which means circuit paths not much thicker than single atoms.

By using 3-D Tri-Gate technology, Gate electrode controls silicon fin from three sides providing improved sub-threshold slope. Therefore, inversion layer area increased for higher drive current. In addition, Intel development team claimed that the process cost adder is only 2-3%. As shown in Figures 1 and 11(c), the 22 nm 3-D Tri-Gate transistors provide improved performance at high voltage and an unprecedented performance gain at low voltage.

The measurement results show 40% increase in performance at low voltage when compared to 32 nm 2D transistors and consume half the power at the same performance level as 32 nm 2-D transistors.

Intel expects to have the first microprocessor using 22 nm 3-D Tri-Gate transistors (The code named Ivy Bridge) in production by late 2012. One can only imagine what the digital future will hold when technology surrounding something ubiquitous as a transistor leapfrogs.

When Intel got the 22 nm fabrication process to work, getting the right number of transistors to fit in a useable form factor, Moore's Law is safe for another two years, when the fabrication process will use 14 nm nodes.

**4.3. Spintronics.** In conventional electronics theory, charge of electron is used to achieve functionalities for diodes, transistors, electrooptic devices. However, the spintronics technology manipulates electron spin, or resulting magnetism, to achieve new/improved functionalities spin transistors Figure 12(b) [30], memories as shown in Figure 12(a) [31], higher speed, lower power, tunable detectors, and lasers,

bits (Q-bits) for quantum computing. Spintronics has actually been around for years. IBM produced disk drive heads, using giant magnetoresistive (GMR) technology, taking advantage of these properties in 1997. Magnetic random access memory (MRAM) could become the next area where spintronics is incorporated. Ideally, MRAM would be able to store a substantial amount of data, consume little energy, operate at a much faster rate than conventional flash memory, and last forever. Figure 12(b) shows the inject polarized spin from one FM contact; other FM contact is analyzer, and modulates current by modifying spin precession via Rashba effect, Asymmetry-spin-orbit interact.

Finding a replacement for flash technology, which is used in cell phones, memory cards in digital cameras, and other devices, is an urgent business in the semiconductor market. Demand for flash is growing extremely rapidly.

**4.4. Carbon Nanotube (CNT).** As we discuss in the previous section, IBM's approach of using DNA molecules as scaffolding—where millions of carbon nanotubes (CNT) could be deposited and self-assembled into precise patterns by sticking to the DNA molecules—may provide a way to reach sub-22 nm lithography.

In our previous works [32], we elucidated the quantum mechanical nature of the Einstein photoelectric effect in terms of a field-effect transistor (FET) made of Carbon Nanotube (CNT) semiconductors. Consequently, we discovered a surprising low-pass band gap property as shown in Figure 13(a), as opposed to the traditional sharp band-pass band gaps. In other words, there exists a minimum amount of photon energy  $n\hbar\omega$  shining on CNT which is necessary to excite the semiconductor CNT into free electrons. Applying a static magnet along the longitudinal direction as shown in (Figure 13(b), (c)), the conduction electron and holes will be spiral in the opposite direction over the surface reducing the current density and the collision recombination chance will therefore be reduced when travelling from the cathode end to the anode end, driven internally by the asymmetric semiconductor-metal (using Ag & Pd) work functions (Schottky interface effect) for an automatic triode read out.

Our previous works [32] show that CNT semiconductors have band-gap-like characteristics different from the traditional semiconductor. CNT semiconductors have a low-pass band gap, rather than band passing, according to Low Pass Band Gap Theorem of CNT (Szu et al. 2008) [33]:

$$\lambda_{\text{de Broglie}} = \frac{h}{p_{\text{electron}}} = n\pi d_{\text{CNT}} = \lambda_{\text{MWIR}}, \quad n = 1, 2, 3, \dots \quad (5)$$

The combination of micron scale circuit board revolution design and field-effect transistor (FET) made of Carbon NanoTube (CNT) semiconductors is an excellent candidate to further enhance Moore's Law in the next few decades.

**4.5. Single-Atom Transistor.** As the size of transistor keeps shrinking based on what we discuss in this paper, where/when could be the end of Moore's Law?

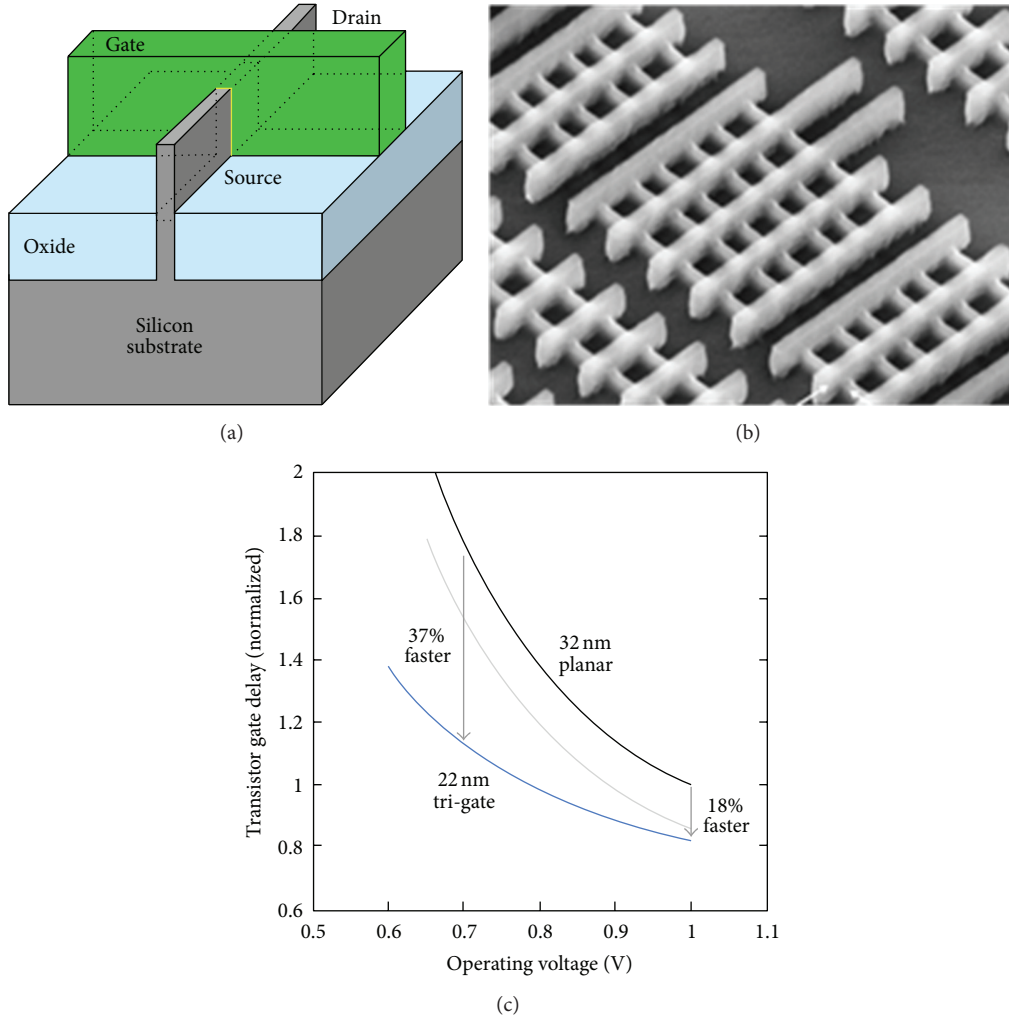


FIGURE 11: Fully depleted Tri-Gate Transistor developed by Intel [5].

Scientists in Australia [34] claim to have created a transistor the size of a single atom, opening the way for the next generation of nanotechnology. The microscopic device is made of a single phosphorus atom embedded into silicon with “gates” to control electrical flow and metallic contacts that are also on an atomic scale. The single atom creation in Australia could radically alter Moore’s prediction, redefining the possible size of future gadgets and their applications. This research team demonstrated a working transistor comprised of a single atom—nearly 100 times smaller than the 22-nanometer cutting-edge transistors fabricated by Intel, as we discussed previously. More importantly, the research team led by Michelle Simmons of the University of New South Wales in Sydney was able to show a method for repeating the process with great accuracy and in a fashion that is compatible with the CMOS technology used in transistor fabrication today.

The work of Simmons and her colleagues could show a way to keep making microprocessor circuitry smaller and smaller through 2020 and beyond. In recent years, advances in quantum computing have offered a viable path to smaller and smaller transistors. But the new research might be the first strong sign that atomic-level transistor fabrication can

be done in keeping with the part of Moore’s Law that is often forgotten amidst the wonderment over tinier and tinier computer chips—that it be done cheaply.

**4.6. Quantum Computers.** Quantum electronic devices and this effect will be more obvious as the transistors are going to have molecular scale.

The theory of quantum computation is one of the possible solutions to move the computation to a different computing paradigm, which is based on the theory of using quantum mechanics to perform computations instead of classical physics [35]. In the quantum world we are faced with a probability density, spread all over the world without a detecting operation, it will be impossible to understand whether that value is zero or one.

As a mathematical definition a Qbit is a vector, a linear combination of two fundamental bases states known as  $|0\rangle = I$  and  $|1\rangle = j$ . A vector presentation is shown as [35]

$$|\varphi\rangle \geq \alpha |0\rangle + \beta |1\rangle, \quad \text{where } \alpha^2 + \beta^2 = 1, \quad (6)$$

where the term  $|x\rangle$  called ket is another representation of a vector, also  $\langle x|$  known as bra is a transposed vector, and

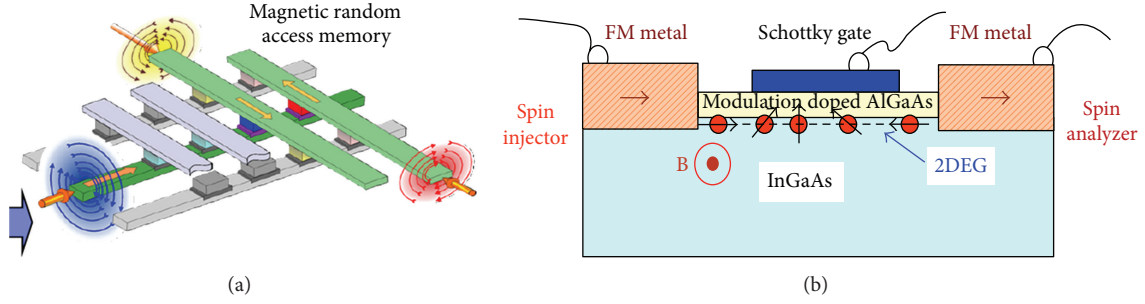


FIGURE 12: (a) Magnetic random access memory (IBM), (b) spin transistor.

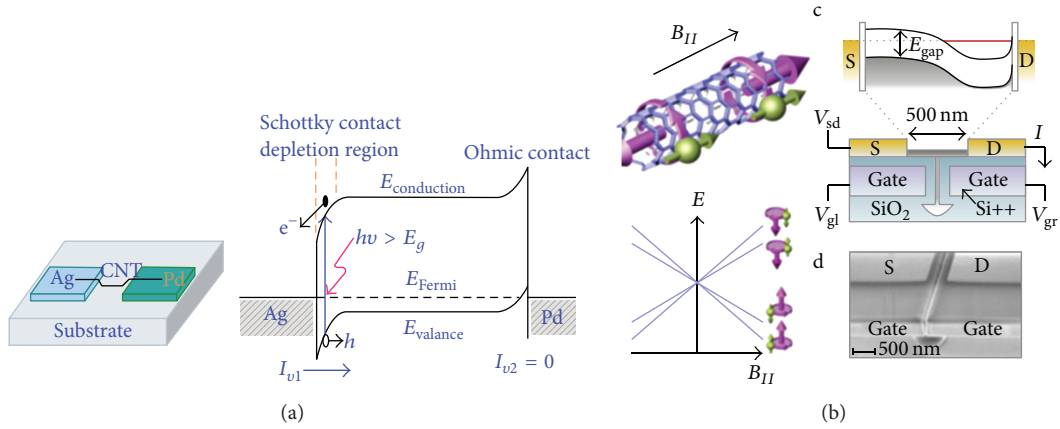


FIGURE 13: (a) 1D CNT has double-bond carbon rigid lattice suffering less thermal noise, which is about 0.5 KT, 1/3 of the thermal noise of CCD dark current liquid nitrogen coolant (LNC). (b) Axial magnetic field increases the surface area as the phase space and avoids the collision recombination of photoelectric carriers (after Rice, Cornell Univ).

$\langle x | y \rangle$  called bracket is the inner product of these two vectors. A vector space with this inner product is called Hilbert Space.

This linear combination is called a Quantum Superposition of the basis states  $|0\rangle$  and  $|1\rangle$ . The only condition with this definition is  $\alpha^2 + \beta^2 = 1$ . This is because  $\alpha^2$  and  $\beta^2$  are quantum probability densities. A sample Qbit model is shown in Figure 14.

Quantum computers are still in the beginning of their way. It has also been suggested that quantum mechanics may be playing a role in consciousness, if a quantum mechanical model of mind and consciousness was developed, this would have significant impact on computational and artificial intelligence. If the brain handles quantum-type transformations somewhere in its neural network this could lead to future quantum computers being biological/biochemical in nature [35].

Although quantum computing can bring our logic element down to molecular scale, however, quantum computers are still faced with the following challenges: (a) interconnection across long distance, (b) room-temperature operation, (c) lack of classical efficient algorithms, (d) setting the initial state of the system, and (e) single defect in line of dots will stop propagation.

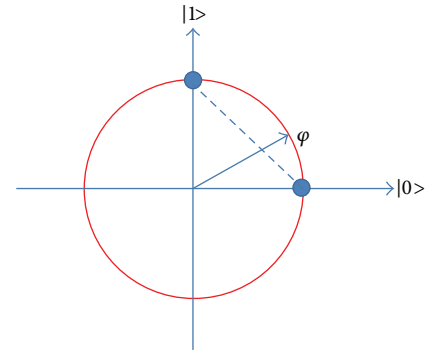


FIGURE 14: Qbit model in state:  $(1/\sqrt{2})|0\rangle + (1/\sqrt{2})|1\rangle$ .

## 5. Summary of Key Technologies

Table 2 shows the summary of key future nanotechnologies with known advantages/disadvantages and application.

## 6. Future of Moore's Law

There have been numerous papers and discussions regarding the lives and deaths of Moore's Law [36]. Before we get into this type of endless debate, we found that we can compare

TABLE 2: Key future nanotechnologies.

Device	Applications	Advantages	Disadvantages
3D transistor	Logic element	Small size	Will still face tunneling effect issue.
	Memory	Low power	Clock tree routing.
Spintronics	Memory	Small size	Control of magnetic field versus spin-polarized current.
	Logic element	Low power	Drivability.
Carbon nanotube FET/graphene	Logic element	Ballistic transport (high speed)	Placement of nanotubes/graphene in a circuit is difficult and not yet production.
		Small size	Control of electrical properties of carbon nanotube (size, chirality) difficult and not yet stably achieved.
Single-electron transistors (SET)	Logic element	Small size Low power	Sensitive to background charge instability.
			High resistance and low drive current. Cannot drive large capacitive (wiring) loads. Requires geometries 10 nm for room-temperature operation.
Quantum dot (quantum cellular automata, QCA)	Logic element	Small size	Multiple levels of interconnection across long distance difficult.
			Room-temperature operation difficult. New computation algorithms required. Method of setting the initial state of the system not available. Single defect in line of dots will stop propagation.
DNA computing	Logic element	High parallelism	Imperfect yield. General-purpose computing not possible.
Quantum computing	Logic element	High computing speed for some certain problem	The coherence in some highly promising concepts for qubits will disappear after about a second. Moreover, the smaller the qubits the faster that process occurs. The information exists may not be long enough to be processed.

the Moore's Law, semiconductor history up to today, and the Dow Jones Industrial Average Curves as shown in Figure 15. What we can learn from this comparison is that people tried their best on both semiconductor developments and the stock market investment in the past few decades. It seems like their curves/trends show us that they are highly related, at least from 1971 up to today (of course we took log on number of transistor). In addition, if we compare that Moore's prediction for the past four decades against the semiconductor industry, we have to admit Moore is a visionary!, no matter what is going to happen in the future.

Looking forward, in this work, we further identify the future transistor counts and places on the following decades, 2020, 2030, and so on. Then, we estimate the sizes of the key technologies that we investigated in this work and locate them on the same chart, assuming Moore's Law is still live. Figure 15 shows that we will face key challenges almost every single decade if we want to meet Moore's Law up to year 2050.

When will Moore's Law end? This is a popular question that scientists keep on asking. To answer this question, we may need to review the original definition of Moore's Law. If we consider Moore's Law as simply just a transistor/component count in a chip, then we can easily break this law today, by making the semiconductor area bigger or

stacking multiple dies in one. Hence, in this work, we consider Moore's Law as a matter of transistor/component density in a chip and focus on the technologies barriers of this law. Based on our calculations along the Moore's Law curve shown in Figure 15, by 2060, our technology node will get into a subatomic scale. In other words, we have nothing to improve on the transistor/component density in a chip. The only thing we can do is extending the chip in 2-D or 3-D (stack) and make the die size larger, unless we find a way to make a switch inside an atom and solve the signal drivability issue also in atom scale in the future! Otherwise, to discuss Moore's Law beyond that point, in Figure 15, will become meaningless.

## 7. Conclusion

Whether there is an ultimate limit to Moore's Law is an open debate dependent upon future electronic innovations, material science, and physics. Moore's prediction as early as 1965 proves since Turing that he is a unique technological visionary who quietly led the silicon revolution with his own law. We have estimated that the potential future nanotechnologies will enhance the current known barriers for Moore's Law. Based on our estimations on the scale of these



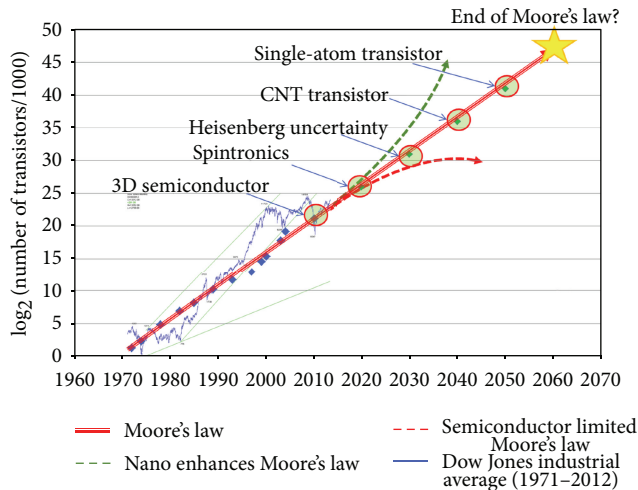


FIGURE 15: Moore's Law history, future, limited factors, and Nano-technology-Enhance factors for Moore's Law and compared with Dow Jones industrial average in the same period of time (1971–2011).

nanotechnologies, we further forecast the major milestones and key technologies that confront us in the near future in Figure 14. The computing industry and the world population have enjoyed five remarkable decades of Moore's Law. Up to the next half-millennium, our discussion of Moore's Law in turn of density of discrete computing elements will become meaningless from quantum mechanical uncertainty and entanglement technologies point of view. As before those days, the economic limit will continue playing the key role, despite of the fact that we know we cannot break the fundamental limits of the atomic and nucleus nature of matter. The ubiquitous computing in the future might be in an entirely different form of the information representation and nonlocal manipulation. However, the bottleneck might be in the transformation between the classical Moore's Law localized computing and a modern Moore's Law-distributed computing that remains to be formulated by some other visionaries.

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